

M-15281US
10/753,673IN THE CLAIMS

The following is a complete listing of the pending claims:

1. (currently amended) A two-transistor PMOS memory cell, comprising:
 - a PMOS select transistor having a drain and a source formed as separate P+ diffusion regions in an N- well;
 - a PMOS floating gate transistor having a drain and a source formed as separate P+ diffusion regions in the N-well, wherein the P+ diffusion region that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source; and
 - an N implant underlying only the P+ diffusion region that forms the floating gate transistor's drain such that an N implant does not underlie either of the P+ diffusion regions forming the select gate's transistor drain and the floating gate's transistor's source.
2. (original) The two-transistor PMOS memory cell of claim 1, wherein the lateral extent of the N implant is substantially the same as the lateral extent of the P+ diffusion region that forms the PMOS floating gate transistor's drain.
3. (original) The two-transistor PMOS memory cell of claim 2, wherein the drain of the PMOS select transistor couples to a bit line of a memory array, and wherein a select gate of the PMOS select transistor couples to a word line of the memory array.
4. (original) The two-transistor PMOS memory cell of claim 2, wherein a floating gate of the PMOS floating gate transistor is formed in a first polysilicon layer, and wherein a

LAW OFFICES OF

MACKESSON KWOK

CHEN & FIELD LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 753-7040
FAX (949) 753-7049

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control gate of the PMOS floating gate transistor is formed in a second polysilicon layer.

5. (original) The two-transistor PMOS memory cell of claim 2, wherein the memory cell includes a single polysilicon layer containing a floating gate of the PMOS floating gate transistor, and wherein a control gate of the PMOS floating gate transistor is formed as a P+ diffusion region in the N- well.
6. (original) The two-transistor PMOS memory cell of claim 2, wherein the memory cell is configured such that the floating gate transistor may be programmed using band-to-band tunneling.
7. (original) The two-transistor PMOS memory cell of claim 2, wherein the memory cell is configured such that the floating gate transistor may be programmed using Fowler Nordheim tunneling.
8. (original) The two-transistor PMOS memory cell of claim 2, wherein the P+ diffusion region that forms the floating gate transistor's drain has a thickness of approximately 0.1 to 0.25 microns.
9. (original) The two-transistor PMOS memory cell of claim 2, wherein the thickness of the N implant underlying the P+ diffusion region that forms the floating gate transistor's drain is approximately 0.1 to 0.25 microns.
10. (withdrawn)

LAW OFFICES OF
MACPHERSON KWOK
CHEW & HEID LLP
2402 Michelson Drive
Suite 210
Irvine, CA 92612
(714) 752-7029
FAX (714) 752-7049

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11. (withdrawn)
12. (withdrawn)
13. (withdrawn)
14. (withdrawn)

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP
2402 Merchant Drive
SUITE 210
Irvine, CA 92612
(714) 753-2010
FAX (714) 752-7049